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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Please cancel claims 8, 20, and 21 without prejudice, amend claims 1, 2, 4, 6, 7, 12, 13, 15, 16, and 22, and add claims 28-30 as follows:

1. (currently amended) A processor with an instruction class controllable pipeline comprising:

a program storage unit holding a diverse plurality of class one and class two executable function instructions, the class one instructions having a first execution latency and the class two instructions having a second execution latency, wherein the first execution latency is shorter than the second execution latency;

~~a~~ an adaptable fetch stage for fetching an instruction from the program storage unit to be stored in an instruction register;

~~a~~ an adaptable decode stage for classifying and decoding the instruction stored in the instruction register and generating an instruction class indication and storing the decoded instruction[[s]] in a decode register;

an adaptable execution stage for execution of [[a]] the decoded instruction stored in the decode register, the decoded instruction being a class one instruction or a class two instruction; and

an adaptable pipeline control unit responsive to the instruction class indication for adapting the latency of ~~a~~ the adaptable fetch stage, the adaptable decode stage, and the adaptable execution ~~pipeline~~ stage dependent on the instruction class indication~~; and~~.

~~an adaptable execution stage for execution of a decoded instruction stored in the decode register, the decoded instruction being a class one instruction or a class two instruction.~~

2. (currently amended) The processor of claim 1, wherein the adaptable fetch stage further comprises:

a program counter and an instruction memory fetch mechanism which are operable to begin instruction processing by fetching one or more instructions from the program storage unit.

3. (previously presented) The processor of claim 1, wherein the executable function instructions comprise:

additions, subtractions, multiplications, divisions, compares, ANDs, ORs, ExclusiveORs, NOTs, shifts, rotates, permutes, bit operations, moves, loads, stores, communications or combinations thereof.

4. (currently amended) The processor of claim 1, wherein the adaptable pipeline control unit further comprises:

a pipeline control mechanism for class one instructions to execute in ~~instructions having~~ the first execution latency; and

a pipeline control mechanism for class two instructions to execute in ~~instructions having~~ the second execution latency.

5. (previously presented) The processor of claim 4 wherein the pipeline control mechanism for class one instructions further comprises:

control for normal pipeline timing for class one instructions, wherein each stage of the normal pipeline has a duration equal to the first execution latency.

6. (currently amended) The processor of claim 4 wherein the pipeline control mechanism for class two instructions further comprises:

an instruction register feedback multiplexer;

a decode register feedback multiplexer;

a program counter and program counter update function;

a hold instruction register signal to control the instruction register feedback multiplexer to hold the contents of the instruction register for the second execution latency upon detection of a class two instruction;

a hold decode register signal to control the decode register feedback multiplexer to hold the contents of the decode register for the second execution latency upon detection of a class two instruction; and

a hold program counter signal to control the program counter update function to hold the contents of the program counter for the second execution latency upon detection of a class two instruction~~; and~~.

~~a control for the adaptable execution stage for the class two instructions to execute instructions having the second execution latency.~~

7. (currently amended) The processor of claim 4 wherein the pipeline control mechanism for class two instructions further comprises:

an instruction register gated clock;

a decode register gated clock;

a program counter gated clock;

instruction register clock gating logic responsive to the instruction class indication to extend the instruction register gated clock period for the second execution latency upon detection of a class two instruction;

decode register clock gating logic responsive to the instruction class indication to extend the decode register gated clock period for the second execution latency upon detection of a class two instruction; and

program counter clock gating logic responsive to the instruction class indication to extend the program counter gated clock period for the second execution latency upon detection of a class two instruction~~; and~~.

~~control for the adaptable execution stage for the class two instructions to execute instructions having the second execution latency.~~

8. (canceled)

9. (previously presented) The processor of claim 1 wherein the adaptable execution stage further comprises:

a class one execution unit operable to execute a class one instruction stored in the decode register, wherein the class one execution unit has the first execution latency; and

a class two execution unit operable to execute a class two instruction stored in the decode register, wherein the class two execution unit has the second execution latency.

10. (original) The processor of claim 1 wherein the decode stage further operates to decode an opcode field to classify an instruction.

11. (original) The processor of claim 1 wherein the decode stage further operates to decode an opcode field and decode of a data type field to classify an instruction.

12. (currently amended) The processor of claim 4 wherein the adaptable pipeline control unit further comprises:

a programmable clock gating mode indicator that specifies a normal clock gating mode and a slow down clock gating mode; and

control for extending pipeline stage timing for both class 1 instructions and class 2 instructions to execute in a longer time period than the second execution latency when the programmable clock gating mode indicator specifies a slow down clock gating mode.

13. (currently amended) A method for processor performance and power optimization of an instruction class adaptable pipeline processor supporting at least two classes of instructions with a first class operable with a first latency for ~~each~~ fetch, decode, and execute pipeline ~~stage~~ stages of the adaptable pipeline and a second class operable with a second latency for ~~each~~ fetch, decode, and execute pipeline ~~stage~~ stages and where, the first latency is shorter than the second latency and where the instructions operable with the first latency can be specified to operate with the first latency or the second latency and where the instructions operable with the second latency can be specified to operate with the second latency, the method comprising:

programming the instruction class adaptable pipeline processor creating an application program containing a mix of two classes of instructions to meet functional requirements with a first plurality of instructions used in the program operable with the first latency specified in a format encoding ~~of each~~ of the first plurality of instructions as class 1 instructions and with a second plurality of instructions used in the program operable with the second latency specified in a format encoding ~~of each~~ of the second plurality of instructions as class 2 instructions;

modifying the application program by changing, where appropriate, the format encodings of class 1 instructions to format encodings that specify the same functionality of the original class 1 instructions but provide class 2 instruction[[s]] indications when decoded to minimize power use while still meeting performance requirements of the application program; and

executing the application program on the instruction class adaptable pipeline processor.

14. (previously presented) A method for processor performance and power optimization of claim 13 further comprises:

appropriately programming a programmable clock gating mode to cause a specifiable majority of the instructions of the class adaptable pipeline processor to execute at a longer latency than the second latency associated with the class 2 instructions, to further minimize power use while still meeting performance requirements of the application program.

15. (currently amended) A very long instruction word (VLIW) processor with a plurality of instruction class controllable pipelines comprising:

a VLIW storage unit holding a diverse plurality of class one and class two executable function instructions located in multiple instruction slot format VLIWs, the class one instructions having a first execution latency and the class two instructions having a longer second execution latency;

~~a~~ an adaptable VLIW fetch stage for fetching a VLIW from a VLIW storage unit to be stored in a VLIW instruction register (VIR);

~~a~~ an adaptable decode stage for classifying and decoding the plurality of executable function instructions stored in the VIR, and generating an instruction class indication for each of the plurality of executable function instructions and storing decoded instructions in a plurality of instruction slot specific decode registers;

a plurality of adaptable execution stages each operable for execution of [[a]] the decoded instruction stored in an instruction slot specific decode register, the decoded instruction being a class one instruction or a class two instruction; and

an adaptable pipeline control unit responsive to the instruction class indications from the classified plurality of executable function instructions for adapting the latency of ~~each~~ the adaptable VLIW fetch stage, the adaptable decode stage, and the plurality of adaptable execution ~~stage~~ stages of the plurality of instruction class controllable pipelines dependent on the instruction class indications~~; and~~.

~~a plurality of adaptable execution stages each operable for execution of a decoded instruction stored in an instruction slot specific decode register, the decoded instruction being a class one instruction or a class two instruction.~~

16. (currently amended) The VLIW processor of claim 15, wherein the adaptable VLIW fetch stage further comprises:

a VLIW memory control unit which is operable to begin VLIW processing by fetching a VLIW from the VLIW storage unit.

17. (previously presented) The processor of claim 15, wherein the executable function instructions comprise:

additions, subtractions, multiplications, divisions, compares, ANDs, ORs, ExclusiveORs, NOTs, shifts, rotates, permutes, bit operations, moves, loads, stores, communications or combinations thereof;

18. (previously presented) The processor of claim 15, wherein the adaptable pipeline control unit further comprises:

a pipeline control mechanism for a VLIW, the VLIW consisting of all class one instructions, to control the execution of the VLIW with the first execution latency; and

a pipeline control mechanism for a VLIW, the VLIW consisting of at least one class two instruction, to control the execution of the VLIW with the second execution latency.

19. (previously presented) The processor of claim 18 wherein the pipeline control mechanism for a VLIW consisting of all class one instructions further comprises:

control for normal pipeline timing for the class one instructions , wherein each stage of the normal pipeline has a duration equal to the first execution latency.

20. (canceled)

21. (canceled)

22. (currently amended) The processor of claim 15 wherein ~~each~~ an adaptable execution stage of the plurality of adaptable execution stages further comprises:

a class one execution unit operable to execute a class one instruction stored in the decode register, wherein the class one execution unit has the first execution latency; and

a class two execution unit operable to execute a class two instruction stored in the decode register, wherein the class two execution unit has the second execution latency.

23-27 (canceled)

28. (new) The processor of claim 1 wherein the latency of the adaptable fetch stage and the latency of the adaptable decode stage are both set equal to the latency of the instruction that is executing in the adaptable execution stage.

29. (new) The processor of claim 1 wherein the adaptable execution stage is a variable duration single-cycle execution stage having a first duration of execution equal to the first execution latency for executing class one instructions and having a second duration of execution equal to the second execution latency for executing class two instructions.

30. (new) A processor with an instruction class controllable execution pipeline comprising:

an instruction register for holding a class one instruction or a class two instruction, the class one instruction belongs to a first group of diverse class one instructions that execute in a time that is less than or equal to a first time period, the class two instruction belongs to a second group of diverse class two instructions that execute in a time that is less than or equal to a second time period, the first single-cycle time period is shorter than the second single-cycle time period;

an adaptable decode stage for classifying and decoding the instruction stored in the instruction register, generating an instruction class indication representing the instruction class of the instruction receive in the instruction register, and storing a decoded instruction in a decode register;

an adaptable execution stage responsive to execute a decoded instruction stored in the decode register, the adaptable execution stage having a first execution logic unit for executing instructions of the first group, a second execution logic unit for executing instructions of the second group; and

an adaptable pipeline control unit responsive to the instruction class indication for adapting the time period of the adaptable decode stage and the adaptable execution stage for decoding and executing an instruction in the first time period for class one instructions and in the second time period for class two instructions dependent on the instruction class indication.